

U.S Application No. 09/788,061  
Amendment dated June 30, 2006  
In Response to Office Action of January 30, 2006

**Amendments to the Claims:**

This listing of claims will replace all prior versions and listings of claims in the application.

1. (original) A wireless communications device, comprising:  
a wireless transceiver; and  
a processor coupled to the wireless transceiver, the processor having a memory comprising a plurality of fragments and an array configured to control the sequence of memory fragments from which data is read.
2. (original) The wireless communications device of claim 1 wherein the processor further comprises a second array configured to indicate a status of each of the memory fragments.
3. (original) The wireless communications device of claim 2 wherein the status indicated by the second array for each of the memory fragments comprises a bit to indicate whether its respective memory fragment is empty.
4. (original) The wireless communications device of claim 1 wherein the processor further comprises a read pointer configured to indicate the memory fragment from which the data is being read.
5. (original) The wireless communications device of claim 1 wherein each of the memory fragments comprises 64 bytes.
6. (original) The wireless communications device of claim 1 wherein the memory fragments comprises 128 memory fragments.

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7. (original) The wireless communications device of claim 6 wherein the array comprises a 128 element array.

8. (original) A processor comprising a memory having a plurality of fragments and an array configured to control the sequence of memory fragments from which data is read.

9. (original) The processor of claim 8 further comprising a second array configured to indicate a status of each of the memory fragments.

10. (original) The processor of claim 9 wherein the status indicated by the second array for each of the memory fragments comprises a bit to indicate whether its respective memory fragment is empty.

11. (original) The processor of claim 8 further comprising a read pointer configured to indicate the memory fragment from which the data is being read.

12. (original) The processor of claim 8 wherein each of the memory fragments comprises 64 bytes.

13. (original) The processor of claim 8 wherein the memory fragments comprises 128 memory fragments.

14. (original) The processor of claim 13 wherein the array comprises a 128 element array.